REMARKS

Claims 1-21 are currently active.

Antecedent support for the limitation of "port cards" is found in original figure 22, now figure 7.

The Examiner has rejected to Claim 5 under 35 U.S.C. 112. Applicants respectfully submit the questioned language is clear and definite. The port cards assemble the packets from the stripes of fragments they receive from the fabrics.

The Examiner has rejected Claims 1-3 as being unpatentable over Cisneros in view of Gaddis and Koehler. In view of the amendments to the claims, applicants respectfully traverse this rejection.

Referring to Koehler, there is disclosed an apparatus and method for synchronization of multiple data paths and recovery from lost synchronization. Koehler teaches that 32-bit data packets are transferred to splitting circuitry 16 which splits each of the data packets into two 16-bit portions which are transferred along to respective parallel paths or pipes on 16-bit buses 18 and 20 for further processing. The splitting circuitry 16 also

generates for each 16-bit portion of the data packet a synchronization code, also referred to as a sync code. As the splitting circuitry splits each data packet into two portions, which are referred to as a high portion and a low portion, it assigns to and couples with each portion a two-bit synchronous code. See column 5, lines 9-26.

Koehler teaches that after the data packets are split by the splitting circuitry, they can be processed by the circuitry that required the packet to be split. Such a circuitry is identified generically in figure 1 as reference numeral 26 and 28. The circuitry 26, 28 can be packet switching circuits that cannot be implemented in 32-bit configurations because of pin count limitations. Thus, Koehler teaches that splitting in regard to the system taught by Koehler, means shortening the size of a the data being sent. See column 5, lines 28-34. This is not striping at all. Furthermore, Koehler fails to teach or suggest the use of fabrics of a switch. The circuitry 26, 28 are switches, not fabrics of switches.

After processing by the circuits 26 and 28, the packet portions are transferred along individual paths to the grouping circuitry 38. The grouping circuitry groups the incoming smaller packet portions back into the originally sized 32-bit packets. See column 5, lines 44-50. Koehler teaches that figure 2 shows the splitting circuitry 16. The 32-bit data packets are received and split into 2 16-bit data streams 42, 44 by a data splitter 46. The 16-bit data packet portions are afforded along the data streams 42, 44 to a high side data

reformatter 52 and a low side data reformatter 54, respectively. The 18-bit data packages, which include the two-bit pcode bits are forwarded out of the splitting circuitry 16 toward the functional circuits 26 and 28. See column 5, line 53-column 6, line 2.

As is evident from the teachings of Koehler and the figures of Koehler, the functional circuits 26, 28 only receive full data from one splitting circuitry 16. There is no teaching or suggestion of each fabric receiving stripes of fragments of packets from each port card as is found in applicants' invention of Claim 1. Accordingly, Koehler does not add anything to Cisneros or Gaddis in relevant part to applicants' invention of Claim 1.

Claim 1 now has the limitation that "the port cards sending stripes of corresponding fragments of each packet to the fabrics". The applied art of record does not teach or suggest anything in regard to striping, or striping of corresponding fragments, let alone sending stripes of corresponding fragments of each packet from each of the port cards to each of the fabrics, as found in Claim 1. At best, the applied art of record shows sending a smaller portion of a packet from a single port card to a single fabric, but nothing at all about stripes of corresponding fragments from more than to more than one fabric. Accordingly, Claims 1-3 are patentable over Cisneros in view of Gaddis and Koehler.

The Examiner has rejected Claims 4-6 as being unpatentable over Cisneros and Gaddis, Koehler and Joffe. Applicants respectfully traverse this rejection. The applied art of record does not teach or suggest the limitations of Claim 1. Claims 4-6 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable.

The Examiner has rejected Claims 7-15 as being unpatentable over Cisneros in view Gaddis. As explained above in regard to Claim 1, Cisneros in view of Gaddis does not teach or suggest Claim 1, as amended. Claim 7 is patentable for the reasons Claim 1 is patentable over the applied art of record. Claims 8-15 are patentable for the reasons Claim 7 is patentable.

The Examiner has rejected Claim 16 as being unpatentable over Cisneros and Gaddis, Koehler and Jones. Applicants respectfully traverse this rejection. Cisneros and Gaddis and Jones do not teach or suggest the limitations of Claim 1 or Claim 7. Claim 16 is dependent to parent Claim 7 and is patentable for the reasons Claim 7 is patentable.

The Examiner has rejected Claims 17-21 as being unpatentable over Cisneros, Gaddis, Koehler, Jones and Joffe. Applicants respectfully traverse this rejection. Claims 17-21 are dependent to parent Claim 7 and are patentable for the reasons Claim 7 is patentable over the applied art of record.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-21, now in this application be allowed.

Respectfully submitted,

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I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 8/11/04

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